

Dual N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
60	0.058 at V _{GS} = 10 V	5.3	13 nC
	0.072 at V _{GS} = 4.5 V	4.7	

FEATURES

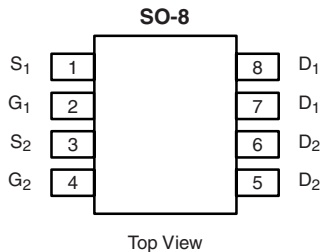
- TrenchFET[®] Power MOSFET

APPLICATIONS

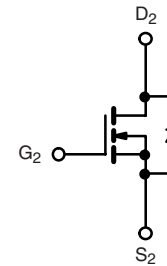
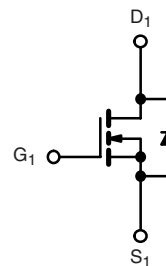
- LCD TV CCFL Inverter



RoHS
COMPLIANT



Ordering Information: Si4900DY-T1-E3 (Lead (Pb)-free)



ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	60	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	5.3	A
		T _C = 70 °C	4.3	
		T _A = 25 °C	4.3 ^{b, c}	
		T _A = 70 °C	3.4 ^{b, c}	
Pulsed Drain Current (10 μs Width)	I _{DM}	20		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	2.6	
		T _A = 25 °C	1.7 ^{b, c}	
Avalanche Current	I _{AS}	11		
Single-Pulse Avalanche Energy	E _{AS}	6.1	mJ	
Maximum Power Dissipation	P _D	T _C = 25 °C	3.1	W
		T _C = 70 °C	2	
		T _A = 25 °C	2 ^{b, c}	
		T _A = 70 °C	1.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, d}	R _{thJA}	55	62.5	°C/W
Maximum Junction-to-Foot (Drain)	R _{thJF}	33	40	

Notes:

- Based on T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 110 °C/W.

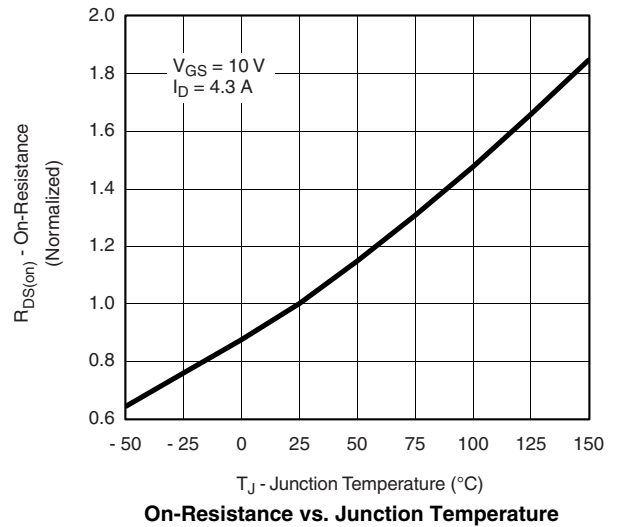
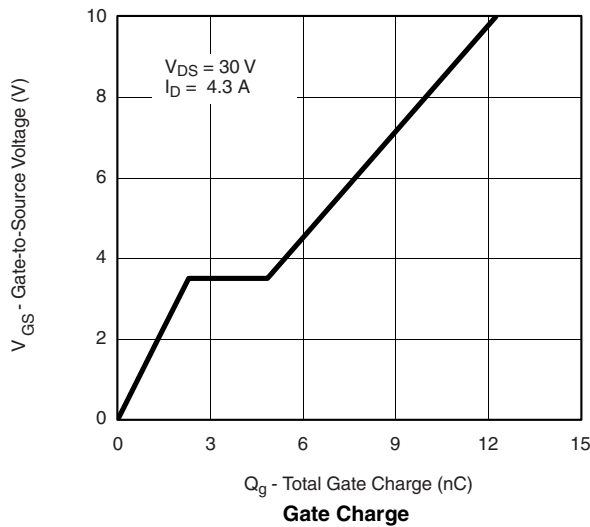
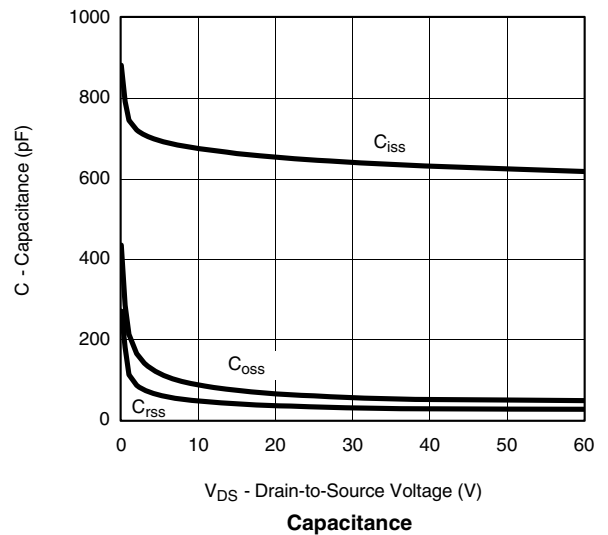
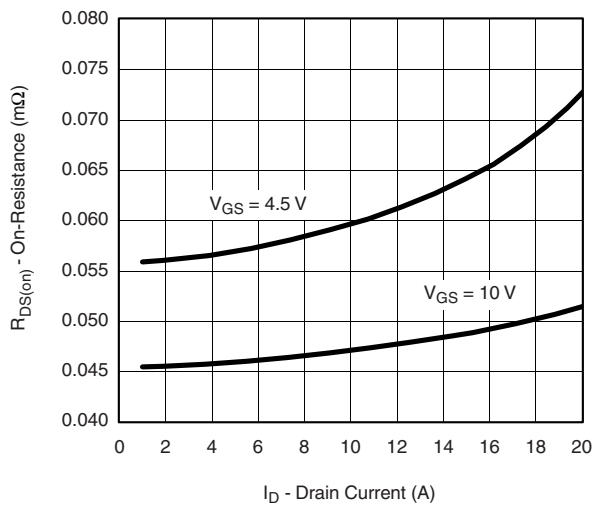
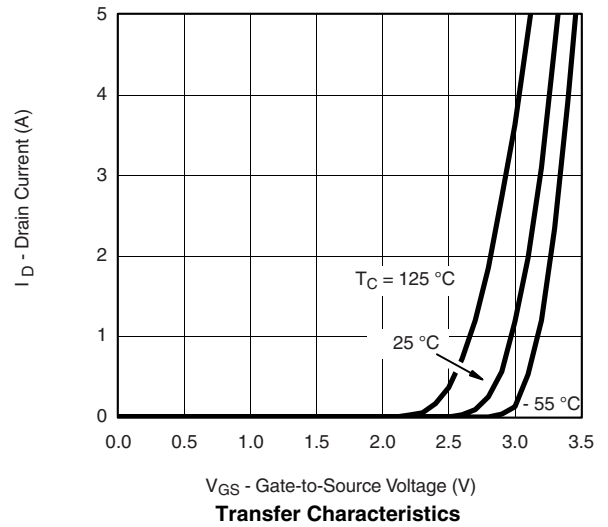
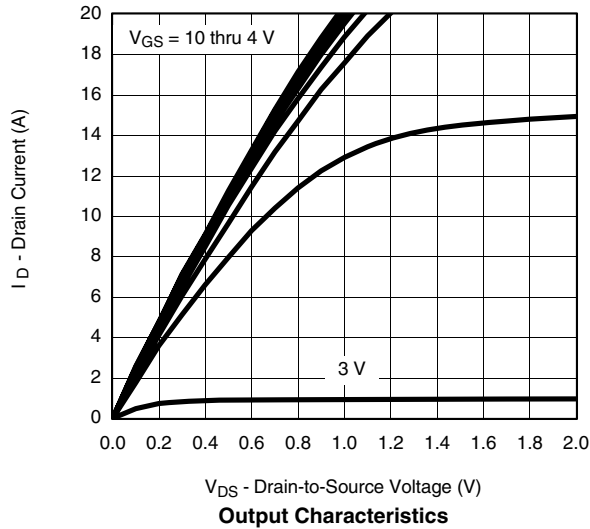
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		55		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1		3	V
		$V_{DS} = V_{GS}, I_D = 5\text{ mA}$		2.5		
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 4.3\text{ A}$		0.046	0.058	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 3.9\text{ A}$		0.059	0.072	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 4.3\text{ A}$		15		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		665		pF
Output Capacitance	C_{oss}			75		
Reverse Transfer Capacitance	C_{rss}			40		
Total Gate Charge	Q_g	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 4.3\text{ A}$		13	20	nC
		$V_{DS} = 30\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 4.3\text{ A}$		6	9	
Q_{gs}			2.3			
Q_{gd}			2.6			
Gate Resistance	R_g	$f = 1\text{ MHz}$		2		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 8.8\text{ }\Omega$ $I_D \cong 3.4\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		15	25	ns
Rise Time	t_r			65	100	
Turn-Off Delay Time	$t_{d(off)}$			15	25	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 8.8\text{ }\Omega$ $I_D \cong 3.4\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		10	15	
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			2.6	A
Pulse Diode Forward Current	I_{SM}				20	
Body Diode Voltage	V_{SD}	$I_S = 1.7\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 1.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		30	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			32	50	nC
Reverse Recovery Fall Time	t_a			25		ns
Reverse Recovery Rise Time	t_b			5		

Notes:

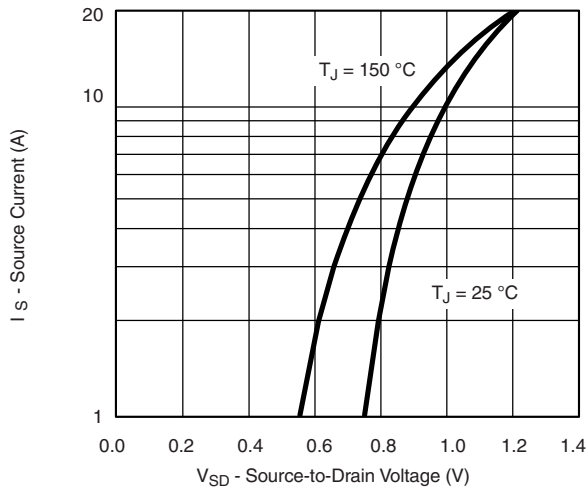
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

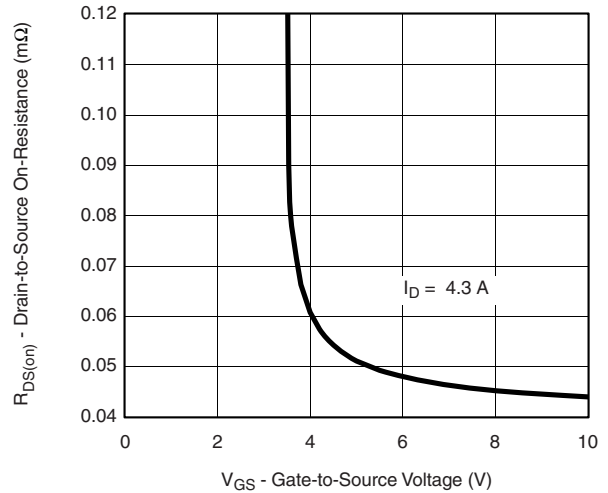
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



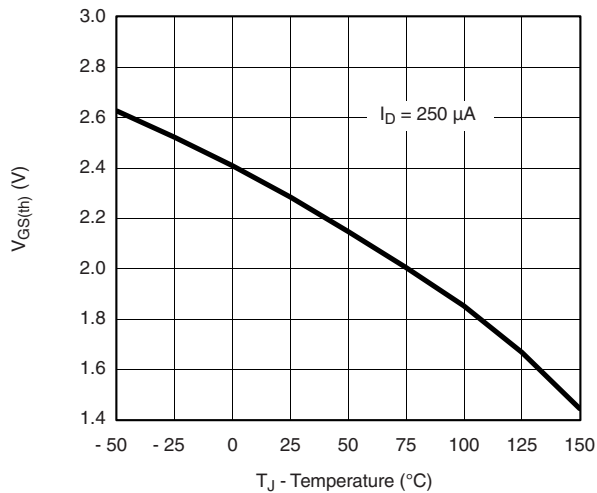
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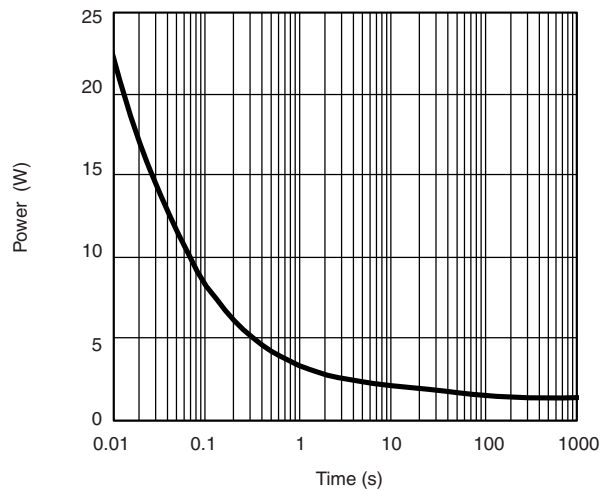
Source-Drain Diode Forward Voltage



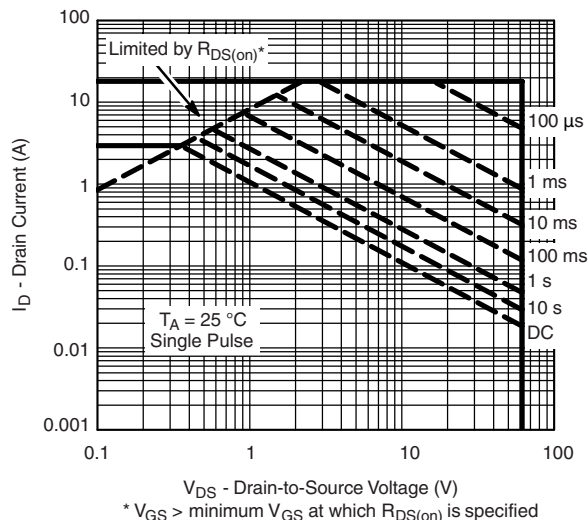
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



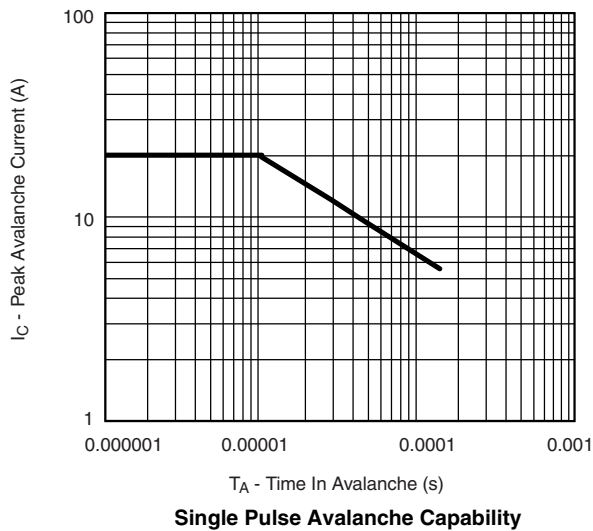
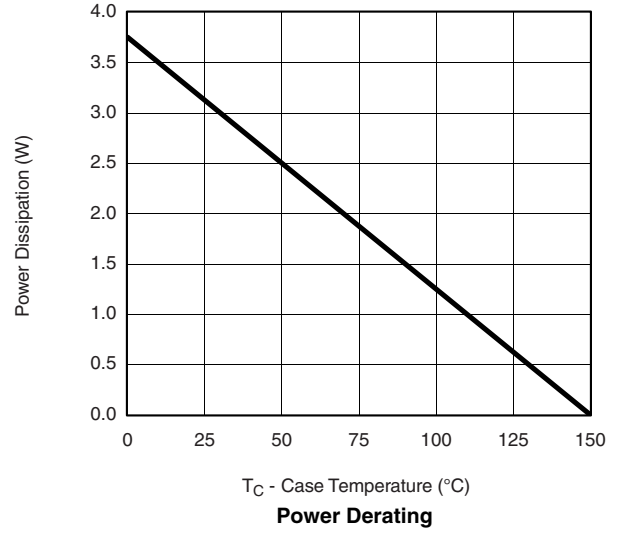
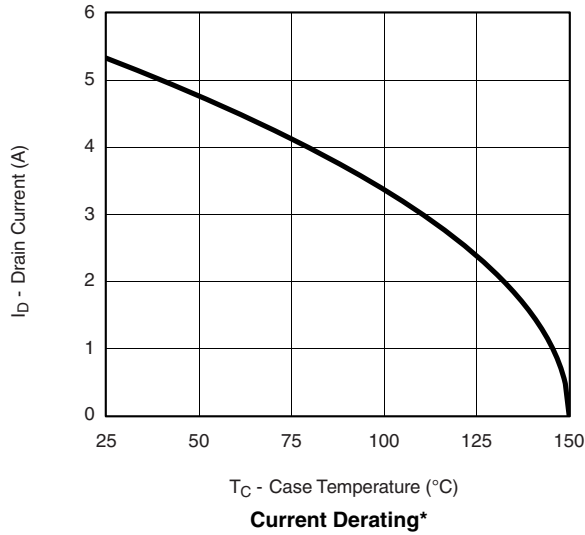
Single Pulse Power, Junction-to-Ambient



Safe Operating Area

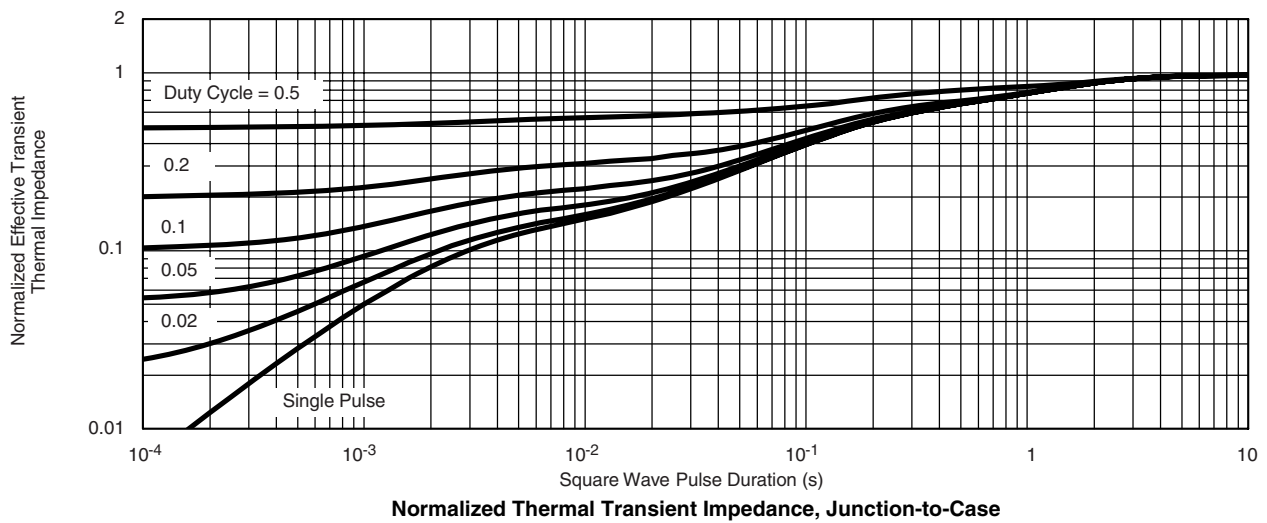
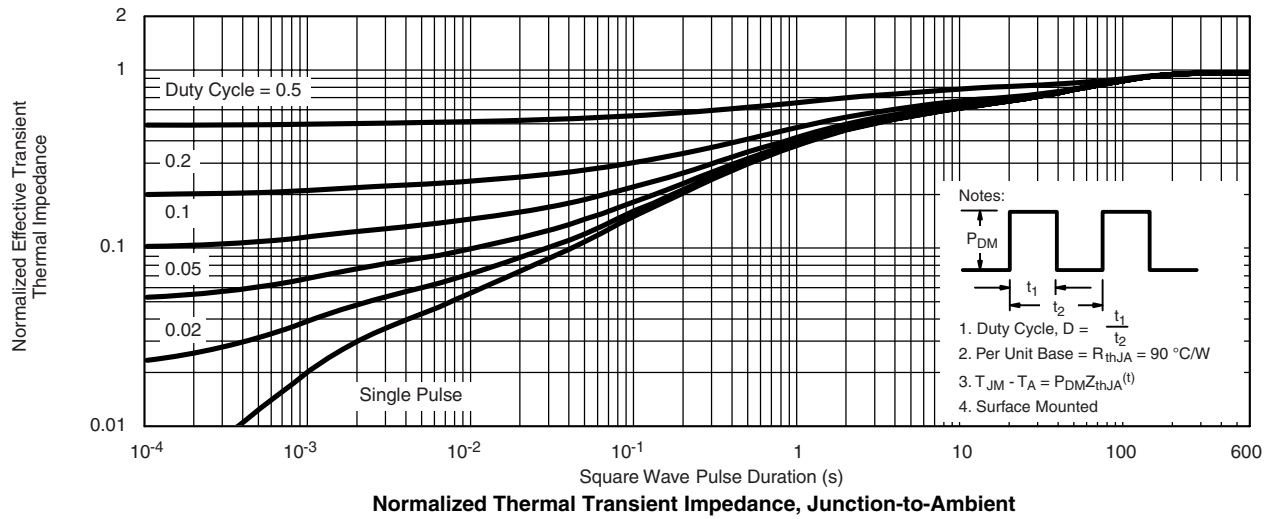
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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